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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,922	07/11/2003	Kazuyuki Yamashita	16810	4232

7590 08/13/2004

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EXAMINER

NGUYEN, VAN THU T

ART UNIT	PAPER NUMBER
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2824

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/617,922

Applicant(s)

YAMASHITA, KAZUYUKI

Examiner

VanThu Nguyen

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. ____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>07/11/2003</u> . | 6) <input checked="" type="checkbox"/> Other: <u>Search Report</u> . |

DETAILED ACTION

1. Claims 1-6 are present for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-2, 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laurent in view of Admitted Prior Art Japanese Patent Laid-Open No. 55130/2002 (APAJP).

Regarding claim 1, Laurent discloses, in FIG. 4, a semiconductor memory device which requires a precharge for a bit line when data is read therefrom, comprising:

a CPU (46);

a precharge duration detector circuit (1) for monitoring a potential on the bit line at the end of a precharge to determine whether or not the potential on the bit line has reached a predetermined potential.

(See column 7, lines 9-13)

However, Laurent does not disclose a control circuit for resetting the operation of the CPU when the potential on the bit line has not reached a predetermined potential.

APAJP discloses, a CPU being reset when it is not operating within a predetermined range of frequency (see page 1, lines 11-21).

Since Laurent and APAJP are both from the same field of endeavor, the purpose disclosed by APAJP would have been recognized in the pertinent art of Laurent.

Art Unit: 2824

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the concept of resetting the CPU when a parameter of a memory device is not operating within the normal range for the purpose of bringing the memory device back to its normal operating range.

Regarding claim 2, Laurent further discloses, in FIG. 1, wherein said precharge duration detector circuit comprises:

a plurality of latch circuits (2A and 2B) each for holding an output signal corresponding to the potential on the bit line associated therewith at the end of the precharge, each said latch circuit switching the output signal based on whether or not the potential on the bit line has reached the predetermined potential at the end of the precharge; and

a logic circuit (10) for operating a logical OR of the output signals from said plurality of latch circuits to deliver the result of the operation as an error detection signal (INRANGE).

(See column 3, line 20 to column 5, line 64)

Regarding claims 5-6, they encompass the same scope of invention as to that of claims 1-2 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Art Unit: 2824

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 3-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Laurent (U.S. Patent No. 6,717,865).

Regarding claim 3, Laurent discloses, in FIG. 4, a semiconductor memory device which requires a precharge for a bit line when data is read therefrom, comprising:

a precharge duration detector circuit (1) for monitoring a potential on the bit line at the end of a precharge to determine whether or not the potential on the bit line has reached a predetermined potential.

(See column 7, lines 9-13)

Regarding claim 4, see above rejection applied to claim 2.

Conclusion


6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2824

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VTN
August 9, 2004


VanThu Nguyen
Primary Examiner
Art Unit 2824